Developing a Readout System for the Sensirion SHT85 Sensors

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This note presents the research and development of a readout system for the Sensirion SHT85 temperature and humidity sensors using the National Instruments sbRIO-9627 CompactRIO readout controller. This system is proposed to be implemented in the RICH detector.

A readout system of up to 48 SHT85 sensors [1] in conjunction with the sbRIO-9627, CompactRIO readout controller [2] is being developed for the RICH detector.

In the test station configured for this development, Fig. 1, three sensors are powered by a 3.3 V power supply. The Tektronix MSO 5204 oscilloscope inspects signal integrity, the Agilent 16902A Logic Analysis System each clock and data line.

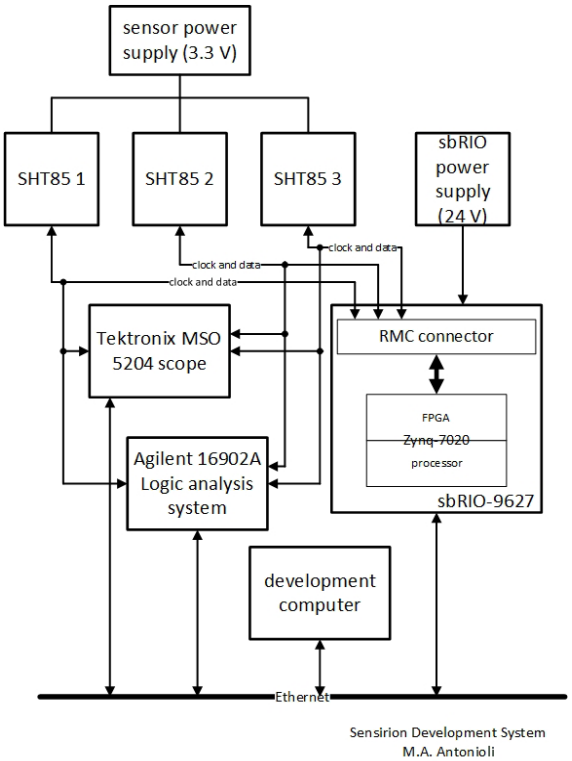

FIG. 1 Development test station.

The FPGA code was written, tested, and debugged for the Xilinx-7020 Zynq processor. The code's main function is to produce independent clock and data signals for each sensor in accordance with the I²C serial computer bus standard [3] and the SHT85 datasheet [4].

The FPGA serves as the master and the sensors as the slaves. The FPGA generates the clock signals, commands, and start and stop conditions that begin and end every data transaction.

Signal level and the timing relationship between the clock and data lines that determine a data transaction conform to the I²C communication standard. Figure 2 shows a typical I²C data transaction.

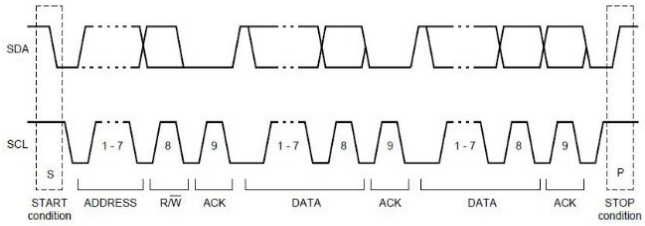

FIG. 2 Timing relation between data and clock.

The serial data (SDA) is the bidirectional data signal between sensor and FPGA. The serial clock (SCL) is the clock signal generated by the FPGA and received by the sensor.

As per the I²C communication standard, each transaction must begin using the start condition and end with the stop condition; if not, an error condition will be detected. Following each data byte that is transmitted by the sensor or the FPGA, an acknowledged (ACK) signal must be sent by the receiver (SHT85 or FPGA) to signify successful reception.

A LabVIEW library† of 18 sub-VI functions, based on the I²C standard functions within a data transaction, was developed, tested, and debugged. Table 1 lists the 18 data transaction functions in the I²C library based on which the LabVIEW library was created.

Additionally, a LabVIEW library of FPGA transactions specific to the SHT85 was developed, tested, and debugged to support the communications of the SHT85 with sbRIO-9627.

To conclude, development of the readout system of SHT85 in conjunction with the sbRIO-9627 has made good progress.

[1] P. Bonneau, et al. *Proposed Integrated Temperature and Humidity Digital Sensor for the RICH Detector*, DSG Note 2019-12, 2019.

[2] P. Bonneau, et al. *Proposed Controller for the Readout of the Temperature and Humidity Digital Sensors Sensirion SHT85 Envisioned for the RICH Detector*, DSG Note 2019-27, 2019.

[3] NXP Semiconductor I²C bus specification and user manual rev.6, April 4, 2014, https://www.nxp.com/docs/en/user-guide/UM10204.pdf.

[4] Sensirion Datasheet SHT85 / D1 Version 1.0, November 2018, https://www.sensirion.com/fileadmin/user_upload/customers/sensirion/Dokumente/0_Datasheets/Humidity/Sensirion_Humidity_Sensors_SHT85_Datasheet.pdf.

† The library can be used by any sensor or instrumentation that complies with the I²C communication standard to form a master/slave data transaction sequence.

Name	Signal Source	Function	Comments
Start condition	master	starts transaction	SDA pulled low while SCL is high
Stop condition	master	ends transaction	SDA pulled high while SCL is high
Address read byte	master	requests slave data	slave's address on bus
Address write byte	master	sends data to slave	slave's address on bus
Command byte	master	sends command to slave	
CRC	slave	data error detection	cyclic redundancy check (CRC)
Read 1 byte	master	master reads slave data byte	
Transmit 1 byte	master	master sends data byte to slave	
Read 1 bit	master	master reads slave data bit	
Transmit 1 bit	master	master sends data bit to slave	
ACK	master or slave	received correct byte	acknowledged required every 8 bits
Write SC	master	Toggles SCL	
Write SDA	master	Toggles SDA	
Set SDA output data	master	Forces SDA state	
Set SDA output enable	master	SDA tri-state control	
Set SCL output data	master	Forces SCL state	
Set SCL output enable	master	SCL tri-state control	
NACK	master or slave	byte not received	not acknowledged

TABLE I. For each of the I^2C function listed in the table, a LabVIEW library of sub-VI functions were generated.